4-Port HUB Controller Chip with USB NIC CH336

Datasheet

Version: V1.2

https://wch-ic.com

1. Overview

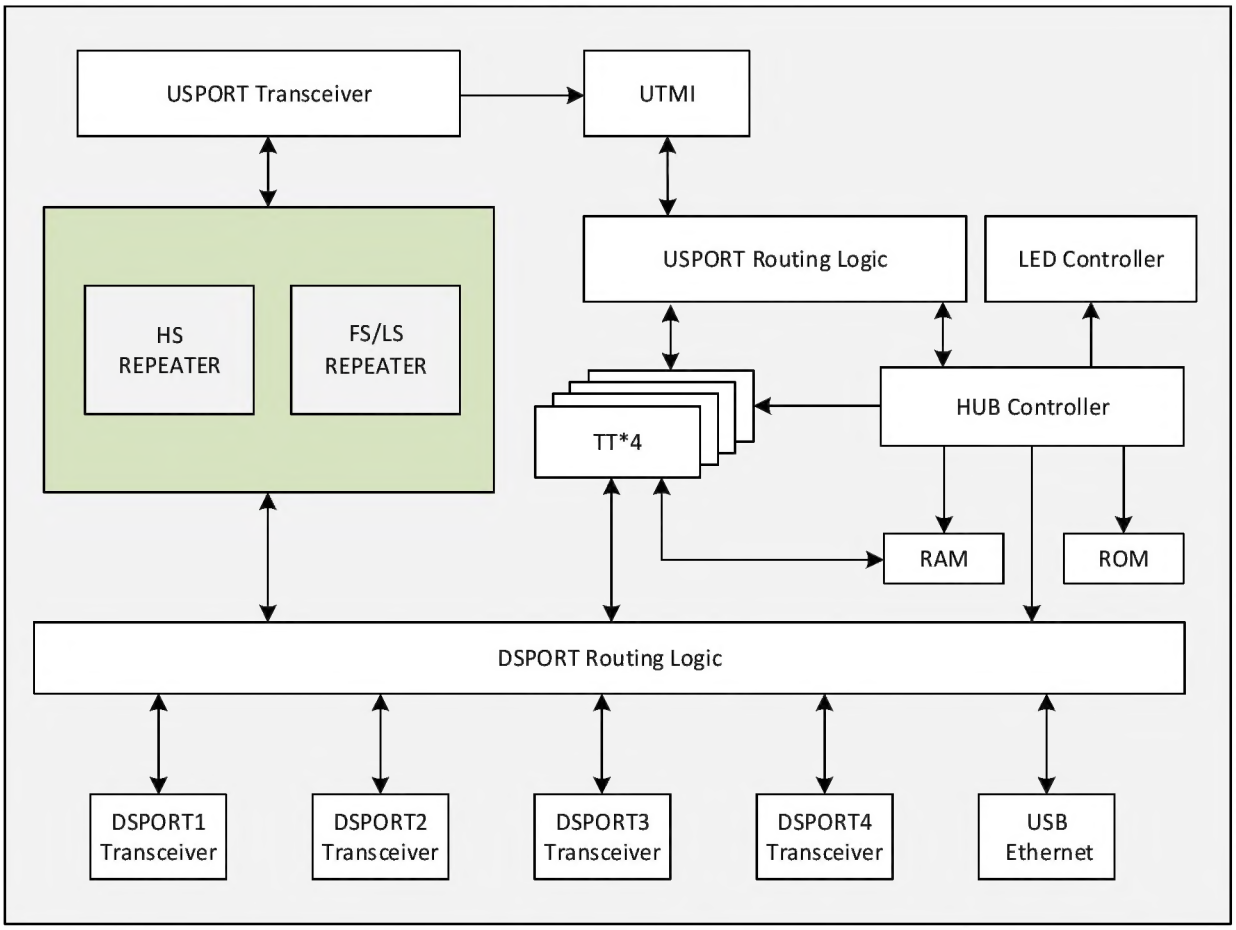
CH336U is a 4-port HUB and USB to Ethernet 2-in-1 controller chip compliant with USB2.0 protocol specification, which integrates 4-port USB HUB and USB 100 Gigabit Ethernet expansion functions in this chip.

CH336F is a 3-port HUB, USB high-speed card reader, USB PD fast charger, and USB to Ethernet 4-in-1 controller chip compliant with USB2.0 protocol specification, which integrates 3-port USB HUB, USB high-speed SD card reader, USB PD fast charger, and USB 100Gb Ethernet expansion.

CH336 upstream port supports USB high-speed and full-speed, downstream port supports USB2.0 high-speed 480Mbps, full-speed 12Mbps and low-speed 1.5Mbps, provides fast direct transmission channel for USB NIC , USB high-speed card reader in HUB. CH336 supports high performance MTT mode, streamlined peripherals, and can be applied to computer and industrial controller motherboards, peripherals, embedded systems and other scenarios.

The following figure is the system block diagram of CH336.

Figure 1-1 System block diagram



The above figure is the internal structure block diagram of the HUB controller system. The HUB controller

mainly consists of three modules: Repeater, TT and controller. The controller is similar to the MCU processor and is used for global management and control. When the upstream port is at the same speed as the downstream port, the routing logic connects the port to Repeater, and when the upstream port is inconsistent with the downstream port, the routing logic connects the port to TT.

TT is divided into single TT and multiple TT, that is, STT and MTT, STT are a single TT core time-sharing scheduling to handle transactions sent by USB hosts to all downstream ports, and MTT refers to multiple TT parallelism, where four TT cores correspond to one downstream port transaction in real time, so MTT can provide full bandwidth for access devices of each downstream port and better support concurrent transmission of multi-port and large amount of data.

Notes:
USPORT Transceiver: Upstream port transceiver PHY;
DSPORT 1-4: Downstream port transceiver PHY;
REPEATER: HUB repeater;
TT: Transaction translator.

2. Features

2.1 USB HUB

- 3/4-port USB HUB, provide 3/4 USB2.0 downstream port, downwards compatible with USB1.1 protocol specifications
- Support high-performance MTT mode and provide independent TT for each port to achieve full-bandwidth concurrent transmission. The total bandwidth is 4 times that of STT.
- Self-developed dedicated USBPHY, low-power consumption technology, support self-power supply or bus power supply
- Provide crystal oscillator, support external clock input, built-in PLL provides 480MHz clock for USB PHY
- Non-Ethernet applications can support crystal-free mode, saving external crystals and capacitors
- The upstream port has built-in 1.5KΩ pull-up resistor, and the downstream port has built-in pull-down resistance required by the USB Host, streamlined peripherals.

2.2 USB Extended NIC and USB High-speed Card Reader

- Built-in self-developed 10M/100M Ethernet MAC+PHY, compatible with IEEE 802.3 10BASE-T/100BASE-TX
- Support CDC-ECM and CDC-NCM protocols, no installation of drivers or optional vendor drivers
- 10M/100M automatic negotiation, support UTP CAT5E, CAT6, support Auto-MDIX, automatically identify positive and negative signal lines
- Support hibernation mode and low-power sleep mode, support network low-power configuration and dynamic power management
- Support remote wake-up through events such as magic packets and network wake-up packets
- Support IPv4/IPv6 packet verification, IPv4 TCP/UDP/HEAD and IPv6 TCP/UDP packet verification generation and inspection
- Support SD and MMC cards and converts them to standard USB mass storage class devices
- Provide SDIO interface, compatible with SD card specification 2.0, compatible with MMC specification 4.5

2.3 USB PD Fast Charging

- Support USB PD2.0/3.0 protocol
- Support maximum 100W external output
- Support USB Type-C forward and reverse plug detection and automatic switching
- Support VDM negotiation to make the device enter Alternate Mode output DP signal
- Support 28V high voltage PDHUB and docking station by adding Type-C interface chip CH211

2.4 Other Features

- Built-in information memory, mass customization of manufacturer or product information and configuration according to the special needs of the industry
- Processor core, high-speed USB, Ethernet and other controllers and PHY transceiver IP is fully self-developed, each module is tightly coordinated, high efficiency and low cost, eliminating IP license fees.
- The built-in LDO linear step-down regulator can convert the USB bus power supply voltage into the 3.3V working power supply of the chip.
- Provide QSOP24, QFN32 and other packaging forms with small size, low cost and easy-to-process.

3. Package

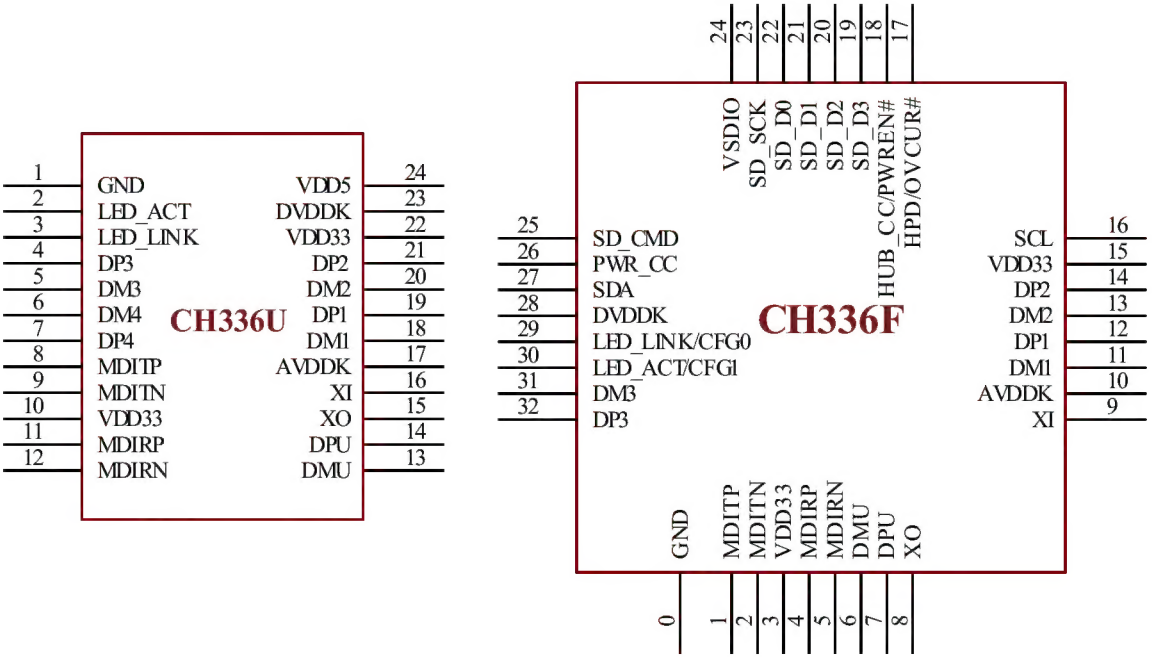


Table 3-1 package description

Package Form	Body Size	Pin Pitch		Package Description	Order Model
QSOP24	3.9*8.7mm	0.635mm	25mil	Quarter Small-Outline Package	CH336U
QFN32	4*4mm	0.4mm	15.7mil	Quad Flat No-leads Package	CH336F

4. Pins

Figure 4-1 Pin definition

Pin No.		Pin name	Type(1)	Function description
CH336U	CH336F			
14	6	DMU	USB	Upstream port USB2.0 signal line D-
13	7	DPU	USB	Upstream port USB2.0 signal line D+
18	11	DM1	USB	1# Downstream port USB signal line D-
19	12	DP1	USB	1# Downstream port USB signal line D+
20	13	DM2	USB	2# Downstream port USB signal line D-
21	14	DP2	USB	2# Downstream port USB signal line D+
5	31	DM3	USB	3# Downstream port USB signal line D-
4	32	DP3	USB	3# Downstream port USB signal line D+
6	-	DM4	USB	4# Downstream port USB signal line D-
7	-	DP4	USB	4# Downstream port USB signal line D+
16	9	XI	I	The input end of the crystal oscillator is connected to one end of the external crystal
15	8	XO	O	The inverted output end of the crystal oscillator is connected to the other end of the external crystal
24	-	VDD5	P	LDO power input, 5V or 3.3V, external 1uF or greater

				capacitor
22	3、15	VDD33	P	LDO output, analog and I/O power input, rated 3.3V, external 1uF or larger capacitor
10	-	VDD33	P	Ethernet power input, external 1uF or larger capacitor, external short to V_{DD33} on pin 22 is required.
-	24	VSDIO	P	Decoupling terminal of the internal power supply of the SDIO pin with an external 0.1uF decoupling capacitor.
17	10	AVDDK	P	Analog core power supply, external 1uF decoupling capacitor
23	28	DVDDK	P	Digital core power supply, external 0.33~1uF decoupling capacitor
1	0	GND	P	Common grounding terminal
8	1	MDITP	ETH	The differential transmitter of 10BASE-T/100BASE-TX in MDI mode; The differential receiver of 10BASE-T/100BASE-TX in MDIX mode.
9	2	MDITN	ETH	
11	4	MDIRP	ETH	The differential receiver of 10BASE-T/100BASE-TX in MDI mode; The differential transmitter of 10BASE-T/100BASE-TX in MDIX mode.
12	5	MDIRN	ETH	
2	30	LED_ACT	O	ETH port status LED 0
3	29	LED_LINK	O	ETH port status LED 1
-	30	CFG1	I	Chip function configuration pin 1.
-	29	CFG0	I	Chip function configuration pin 0。
-	22	SD_D0	I/O	SDIO interface data pin 0.
-	21	SD_D1	I/O	SDIO interface data pin 1.
-	20	SD_D2	I/O	SDIO interface data pin 2.
-	19	SD_D3	I/O	SDIO interface data pin 3.
-	23	SD_SCK	O	SDIO interface clock pin.
-	25	SD_CMD	O	SDIO interface command pin.
-	26	PWR_CC	5I/O	The external power supply terminal PD protocol communication pin CC is used to connect the Type-C power adapter.
-	18	HUB_CC/ PWREN#	I/O	PD enable mode: the communication pin of upstream port PD protocol is used to connect USB hosts such as mobile phones/computers. *Note: When PD is enabled, the power output control pin of the downstream port is provided by CH211.* PD disable mode: Downstream port power output control pin, turned on at low level.
-	27	SDA	I/O	The data signal line of 2-wire serial interface is used to connect CH211 chip.
-	16	SCL	I/O	The clock signal line of 2-wire serial interface is used to connect CH211 chip.
-	17	HPD/ OVCUR#	I	PD enable mode: HPD detection pin. PD disable mode: Downstream port overcurrent detection input pin, low level overcurrent.

Note 1: Pin type abbreviations:

USB = USB signal input;

ETH = Ethernet signal pin;

I = 3.3V signal input;

O = 3.3V signal output;

5I = Rated 3.3V signal input, support 5V tolerant voltage;

P = Power or ground.

5. Function Description

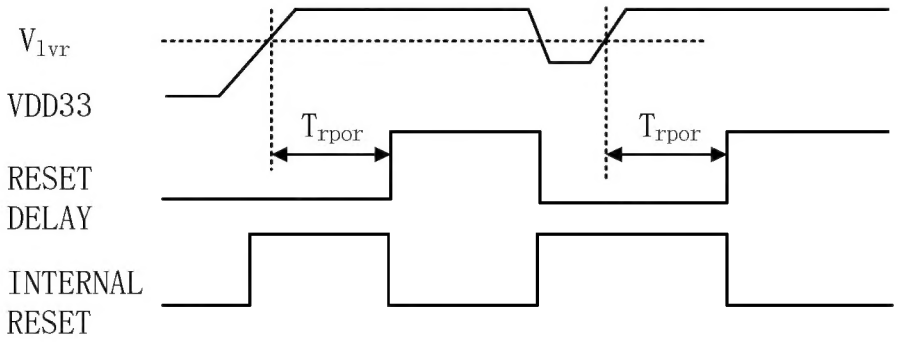
5.1 Reset

The chip is embedded with a power-on reset module, and in general, there is no need to provide an external reset signal.

5.1.1 Power-on Reset

When the power supply is powered on, the POR power-on reset module in the chip will produce a power-on reset sequence and delay the Trpor about 25ms to wait for the power supply to stabilize. In the process of operation, when the power supply voltage is lower than Vlvr, the LVR (low voltage reset) module in the chip will produce a low voltage reset until the voltage picks up, and delay to wait for the power supply to stabilize. Figure 5-1 below shows the power-on reset process and the low-voltage reset process.

Figure 5-1 Reset during power-up



5.2 Bus Power Supply and Self-power Supply

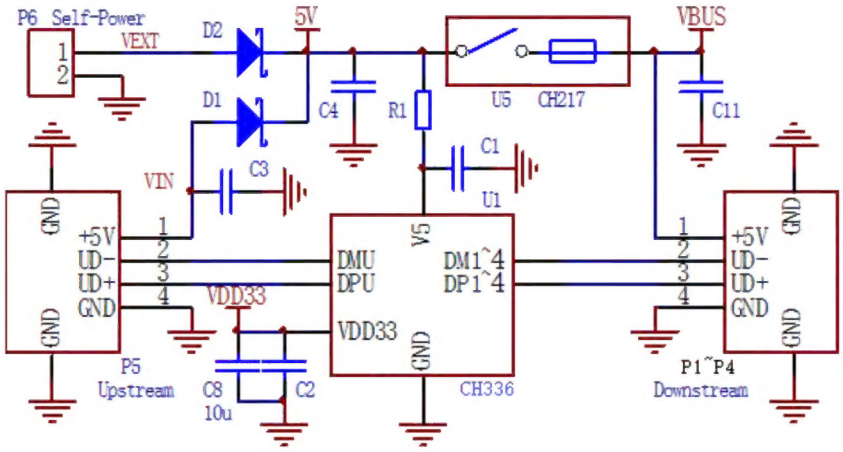
CH336 supports self-powered mode. The bus power supply comes from the upstream port of USB, and the power supply capacity is 500mA or 900mA, 1.5A and other standards. The internal resistance loss of USB wire and the consumption of HUB itself will reduce the power supply capacity of the downstream port, and the voltage of the downstream port may be on the low side. Self-power supply usually comes from an external power port, depending on the power supply capacity of the external power supply.

Since it is difficult for the self-powered and bus-powered voltages to be exactly equal, the HUB needs to avoid generating large currents by directly shorting the two. In addition, when the USB upstream port is disconnected, the HUB should also avoid the self-powered external power supply backing up current to the USB bus and USB host.

5.2.1 Bidirectional Isolation Schematic

Diodes D1 and D2 are used to bidirectionally isolate the V_{BUS} bus power supply and the P6 port external power supply to prevent the 2 power supplies from flowing back to each other. High-power Schottky barrier diodes are used to reduce their own voltage drop. The downstream port V_{BUS} gets a voltage of 4.7V or even lower, only for indication.

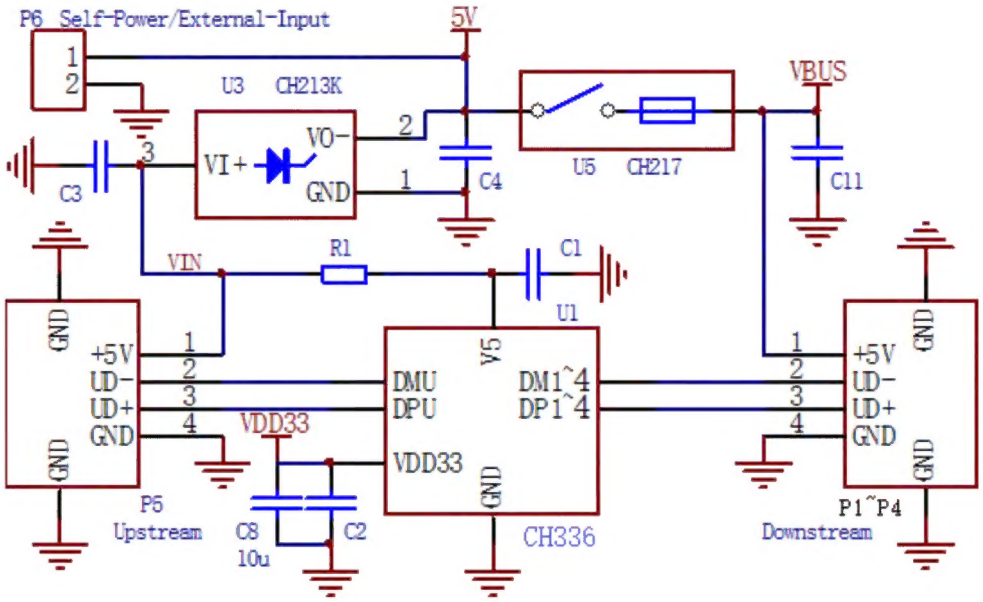
Figure 5-2 Schematic diagram of Schottky barrier diode bidirectional isolation of V_{BUS} and external power supply



5.2.2 Practical Single Isolation Solution

The function of the ideal diode is low drop unidirectional conduction, and U3 is used to avoid the external power supply from port P6 backing up to the upstream port V_{BUS}. At 500mA current, the voltage drop of U3 is about one-third of that of the Schottky barrier diode, and the downstream port V_{BUS} can get a voltage of 4.9V.

Figure 5-3 Schematic diagram of ideal diode isolating V_{BUS} and external power supply



5.3 USB to Ethernet Function

The CH336 chipset integrates USB to 100Gb Ethernet functionality with an integrated 10M/100M Fast Ethernet MAC controller and transceiver PHY that is compatible with the IEEE 802.3 10Base-T, 100Base-TX protocol standard. Supports auto-negotiation and Auto-MDIX, providing the necessary features for transmission over CAT5 and CAT6 network cables. Built-in 50Ω impedance matching resistor with streamlined peripheral circuitry.

ETH related feature pins are as follows:

Table 5-1 Description of Ethernet function pins

Pin name	Type	Function description
MDITP	ETH	Differential transmitter of 10BASE-T/100BASE-TX in MDI mode

MDITN	ETH	Differential receiver of 10BASE-T/100BASE-TX in MDIX mode
MDIRP	ETH	Differential receiver of 10BASE-T/100BASE-TX in MDI mode
MDIRN	ETH	Differential transmitter of 10BASE-T/100BASE-TX in MDIX mode
LED_ACT	O	ETH port status LED 0
LED_LINK	O	ETH port status LED 1

The Ethernet controller supports IPv4/IPv6 packet check, IPv4TCP/UDP/HEAD and IPv6TCP/UDP packet check generation and inspection. Support IEEE802.3x-compliant flow control and half-duplex collision pressure fallback flow control. VLAN tags that conform to the IEEE802.3Q standard are supported. Support Magic packet Wake up, optional low-power consumption in hibernation mode, automatic power management, can save power consumption in no-load or light load, and support 10Base-T energy saving mode.

The chip supports CDC-ECM mode by default, and custom firmware can support vendor drivers and CDC-NCM. The firmware will select and enable the corresponding mode according to the configuration requirements of the user and the commands issued by the host computer of PC. Support to configure relevant parameters through built-in EEPROM, including MAC address, MAC filter configuration, USB manufacturer ID, product ID, USB power configuration and manufacturer custom string and other information.

5.4 USB to High-speed Card Reader Function

CH336F chip integrates USB to high-speed card reader function, and supports SD card and MMC card. Realize the conversion of storage media such as SD card or MMC card into standard USB mass storage devices.
Related function pins are as follows:

Table 5-2 Card reader function pin description

Pin name	Type	Function description
SD_D0	I/O	SDIO interface data pin 0.
SD_D1	I/O	SDIO interface data pin 1.
SD_D2	I/O	SDIO interface data pin 2.
SD_D3	I/O	SDIO interface data pin 3.
SD_SCK	O	SDIO interface clock pin.
SD_CMD	O	SDIO interface command pin.

5.5 Functional Configuration

Some functions of CH336 chip can be configured in 2 ways: built-in EEPROM and I/O configuration pins. The parameter configuration function of internal EEPROM takes precedence over the pin configuration function. Configuration pins are generally multiplexing pins, which are used as configuration pins during reset, and then switched to corresponding functional pins after reset.

CH336F chip has built-in 3-port HUB function, USB card reader function, USB 100 MB network card function and PD fast charging function, which supports overall overcurrent detection and overall power control. Among them, USB card reader function, USB extended Ethernet function and PD fast charging function can be configured through configuration pins.

Table 5-3 CH336F configuration pin description

Configuration pin		Function enable/disable description		
PIN30	PIN29	USB card reader function	USB to Ethernet function	PD fast charging function
CFG1	CFG0			
0	0	×	√	√
0	1	√	√	×

1	0	√	×	√
1	1	√	√	√

6. Parameters

6.1 Absolute Maximum Value (Critical or exceeding the absolute maximum value will probably cause the chip to work improperly or even be damaged)

Name	Parameter Description	Min.	Max.	Unit
T_A	Ambient temperature during operation	0	70	℃
T_S	Ambient temperature during storage	-55	150	℃
V_{DD5}	LDO input power voltage (V_{DD5} pin is connected to power supply, GND pin is connected to ground)	-0.4	5.8	V
V_{DD33}	Working power supply voltage (V_{DD33} pin is connected to power supply, GND pin is connected to ground)	-0.4	4.0	V
V_{USB}	Voltage on USB signal pin	-0.4	V_{DD33}+0.4	V
V_{GPIO}	The voltage on other (3.3V) input or output pins	-0.4	V_{DD33}+0.4	V
V_{ESDIO}	HBM ESD tolerant voltage on other pins	2K		V

6.2 Electrical Parameters (Test conditions: CH336U, T_A=25℃, V_{DD5}=5V or V_{DD33}=3.3V)

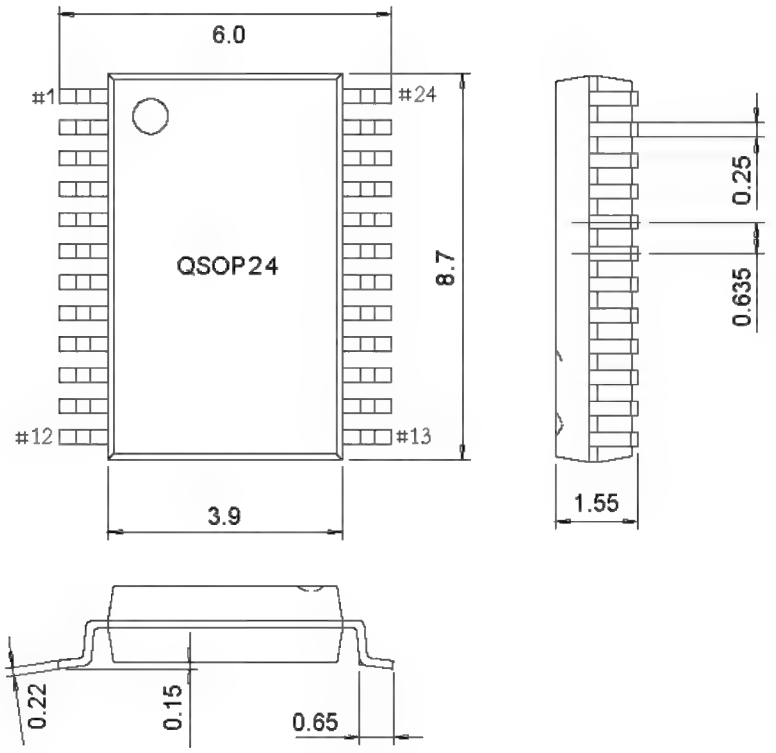
Name	Parameter Description			Min.	Typ.	Max.	Unit
V_{DD5}	LDO input power voltage @V_{DD5}		Enable internal LDO	3.8	5.0	5.5	V
V_{DD33}	LDO output voltage @V_{DD33}		Enable internal LDO	3.2	3.3	3.4	V
	External supply 3.3V voltage @V_{DD33}		No need internal LDO	3.2	3.3	3.4	
I_{LDO}	Internal power regulator LDO external 3.3V load capacity					100	mA
I_{CC}	Working current	Upstream high-speed	4 downstream high-speed + ETH		154		mA
		Upstream high-speed	1 downstream high-speed + ETH		112		mA
		Upstream high-speed	4 downstream full-speed + ETH		104		mA
		Upstream full-speed	4 downstream full-speed		34		mA
		Upstream high-speed Upstream full-speed	Downstream no device Including 1.5KΩ pull-up		0.56		mA
I_{SLP}	Deep sleep power current (Excluding 1.5KΩ pull-up) Or: Self-sleep power supply current (Without USB host)				0.34		mA
V_{IL}	Low level input voltage		Standard I/O pin	0		0.8	V
V_{IH}	High level input voltage		Standard I/O pin	2.0		V_{DD33}	V
V_{OL}	Low level output voltage		Sink current 5mA		0.4	0.6	V
V_{OH}	High level output voltage		Source current 5mA	V_{DD33}-0.6	V_{DD33}-0.4		V
R_{PU}	Pull-up equivalent resistance			30	40	55	kΩ
R_{PD}	Pull-down equivalent resistance			30	40	55	kΩ
V_{lvr}	Voltage threshold for low voltage reset of power supply			2.4	2.9	3.2	V

7. Package

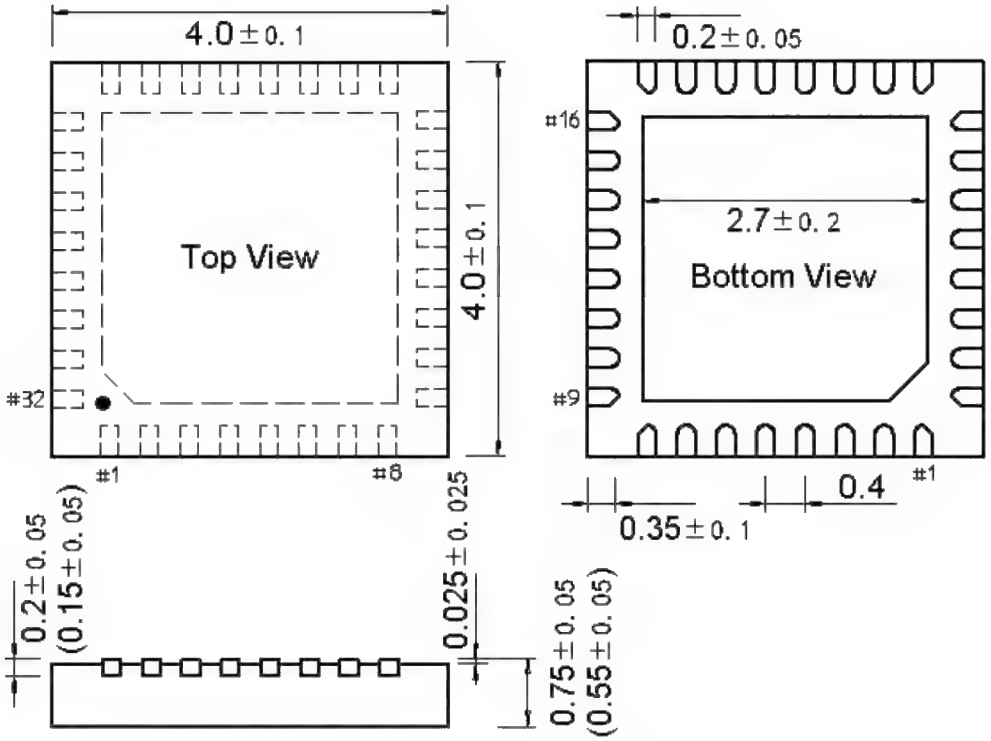
Note: All dimensions are in mm (millimeters).

The pin center spacing values are nominal values, with no error. Other than that, the dimensional error is not greater than the greater of ±0.2mm.

7.1 QSOP24



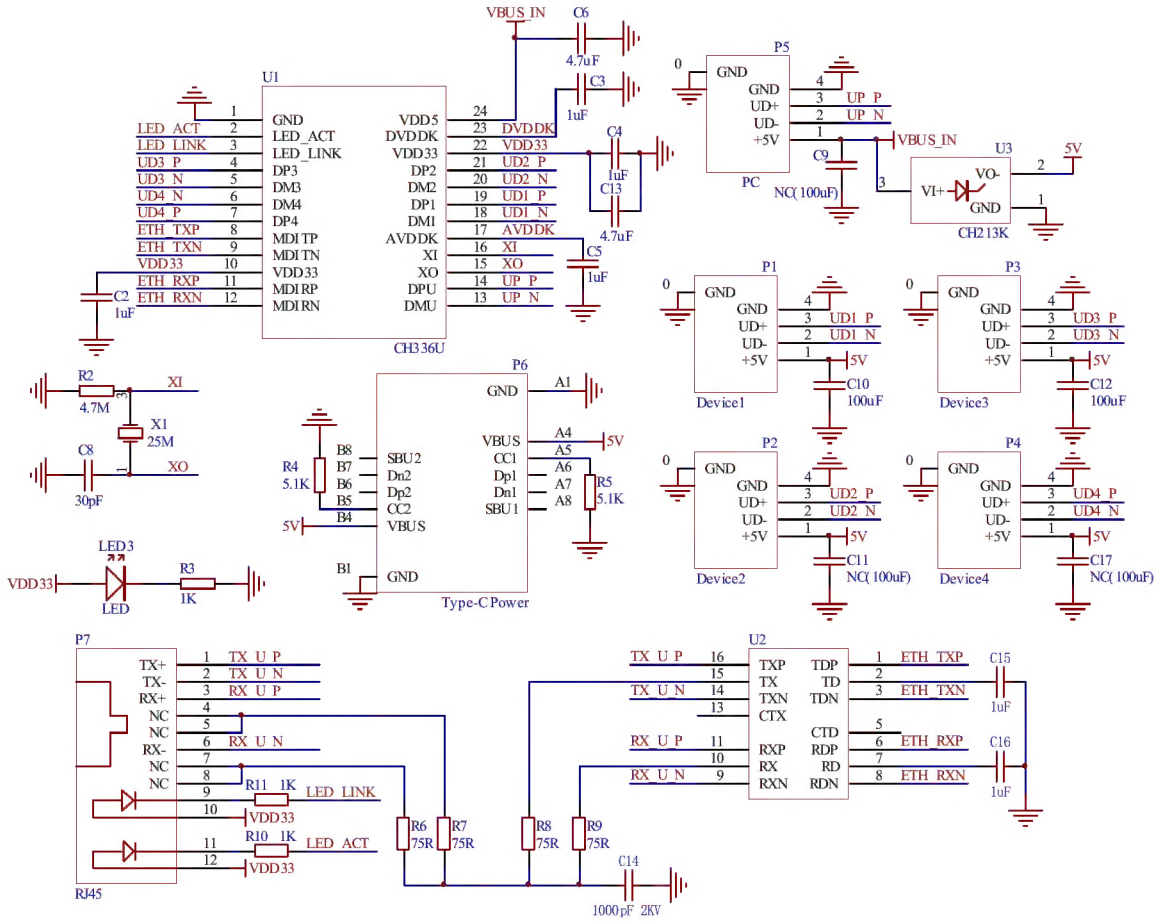
7.2 QFN32


4.0±0.1
Top View
4.0±0.1
#32
#1
#8
0.2±0.05
(0.15±0.05)
0.025±0.025
0.75±0.05
(0.55±0.05)
0.2±0.05
#16
2.7±0.2
Bottom View
#9
#1
0.4
0.35±0.1

8. Application

8.1 HUB Application with USB NIC

Figure 8-1 Reference circuit diagram for CH336U application



In the figure above, P1-P4 is the four downstream USB interfaces of HUB, P5 is the upstream USB interface of HUB, P6 is the external power supply interface, and P7 is the Ethernet RJ45 interface.

U2 is a network transformer, U3 is an ideal low-voltage drop diode CH213, with simple over-current and short-circuit protection functions, and faster protection response, used to avoid upstream port P5 V_{BUS_IN} backflow of P6 external power supply, especially when the upstream port such as the computer is turned off and the P6 external power supply is still supplied. Theoretically, U3 can be replaced by Schottky barrier diodes, but it is necessary to choose devices with low voltage drop, otherwise the output voltage of downstream port V_{BUS} will be reduced. When 300mA load current, the voltage drop of Schottky barrier diode is about 0.3V, and that of ideal diode is about 0.05V.

At the moment when the USB device in the downstream port is hot-plugged, the dynamic load may instantly drop the V_{BUS} and 5V voltage, which may lead to the LVR, resulting in the disconnection and reconnection of the whole HUB. Improvement methods: (1) Increase the electrolytic capacitor of 5V power supply (Increase the

capacity of C9 or C6 shown in the specification) to alleviate the drop; (2) Increase the power capacitance of HUB chip (Increase the capacity of C13 shown in figure, such as 22uF); (3) Enhance the power supply capacity of 5V or change to self-power supply, in addition, improving the quality of USB wire will also improve the power supply capacity.

The actual working current carrying capacity should be considered when designing the PCB. The PCB of the V_{BUS_IN}, 5V and P6 and the GND routing paths of each port should be as wide as possible. If there are holes, multiple parallel connections are recommended. The D+ and D- signal lines of the USB port are arranged in parallel according to the high-speed USB specification to ensure the characteristic impedance and provide ground wires or copper cladding on both sides as far as possible to reduce the signal interference from the outside.

5V overvoltage protection devices are recommended, and all USB signals are recommended with ESD protection devices, such as CH412K, whose V_{DD33} should be connected to 3V3.

8.2 Type-C/PD 100W Fast Charging Docking Station Application

Figure 8-2 Reference circuit diagram for CH336F Type-C/PD 100W fast charging docking station application

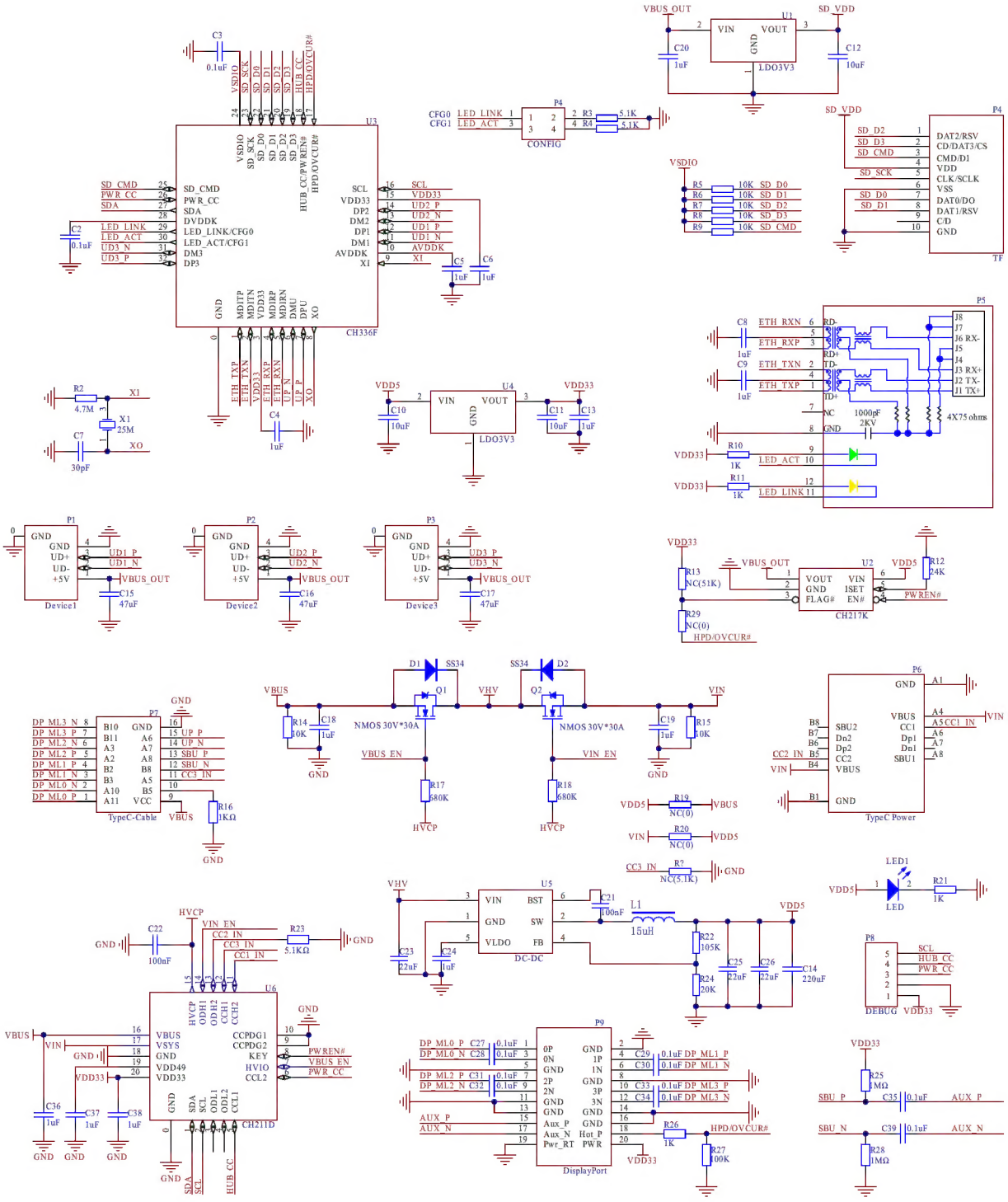


Figure 8-2 above is a reference diagram for CH336F to realize the application of Type-C/PD 100W fast charging docking station, which supports 3-port HUB, USB high-speed card reader, USB to Ethernet and USB PD 100W fast charging function. The PD protocol is implemented by CH336F, which natively supports USB PD2.0/3.0 negotiation, and can charge the maximum power of 100W (20V*5A) while communicating with USB HUB on Type-C interface. CH211D is a Type-C/PD high-voltage interface chip with built-in high-voltage switch and boost module, which provides high-voltage drive with CH336F and supports low-cost N-type MOSFET power switch.

P1-P3 are the 3 downstream USB ports of the HUB, P4 is the SD card port, P5 is the RJ45 port with built-in network transformer, P6 is the pure power supply Type-C port, which is only used for connecting to external power adapter.P7 is the upstream USB port of the HUB, which is usually connected to PC or other USB hosts.P9 is the interface for DP video signals.P7 supports Type-C power role DRP switching, if P6 is connected to external power adapter, then P7 port will work in SRC/DFP mode, this PD docking station transmits the external power to PC for charging, and at the same time provides to DC-DC to generate 5V for VBUS power for USB. If only the PC is connected and no power is supplied to the P6 port, then the P7 port will work in SINK/UFP mode, and this PD docking station applies power from the PC to the DC-DC.

DC-DC will step down the maximum voltage of VHV from 20V to 5V. The DC-DC controller should support full duty cycle output, and the continuous output current should not be less than the actual demand of 3 downstream ports, and it is recommended to be no less than 3A. The internal resistance of MOSFET is recommended not to exceed 16mΩ, so as to reduce the heating when the charging current lasts for 5A. If only 5V*3A is needed, DC-DC can be omitted and the tolerant voltage of MOSFET can be reduced.

If you need to support 28V 140W power or other specific voltage/power fast charging, or bi-directional fast charging, or PD high power fast charging for downstream Type-C port, please contact us.